SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Kenichi Hamada, a citizen of
Japan residing at Kawasaki, Japan, Satoshi Furuta, a citizen
of Japan residing at Kawasaki, Japan and Masakazu Taguchi, a
citizen of Japan residing at Kawasaki, Japan have invented
certain new and useful improvements in

CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION
SYSTEM AND AN APPARATUS HAVING A DATA REPRODUCTION
SYSTEM INCLUDING SUCH A CLOCK ADJUSTMENT APPARATUS

of which the following is a specification : -

TITLE OF THE INVENTION

CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION SYSTEM AND AN APPARATUS HAVING A DATA REPRODUCTION SYSTEM INCLUDING SUCH A CLOCK

5 ADJUSTMENT APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to

10 clock adjustment apparatus for data reproduction systems and apparatus having data reproduction systems including such clock adjustment apparatus, and more particularly, to a clock adjustment apparatus for a data reproduction system of a data

15 recording apparatus such as an optical disk apparatus, a magneto-optical disk apparatus or a magnetic disk apparatus, and an apparatus having a data reproduction system including such a clock adjustment apparatus. A magneto-optical disk

20 apparatus, for example, requires an increasingly high recording density of a recording medium, and therefore, needs a data recording/reproduction method with higher accuracy. Adopted as one of such methods is a combination of recording data modulated

25 to a partial response (PR) waveform onto a magneto-optical disk and sampling a readout signal from the magneto-optical disk at a predetermined sampling frequency so as to detect maximum likelihood data through, what is called, the Viterbi decoding

30 detection (or the maximum likelihood sequence estimation: MLSE). Hereinafter, this combination method is referred to as a PRML method.

With respect to the PRML method, it is important to provide phase compensation so that a

35 quantized readout signal can be sampled in synchronism with a clock signal.

2. Description of the Related Art

Regarding a data reproduction system for reproducing recorded data in accordance with the Viterbi algorithm from sampled values obtained by sampling readout data from a recording medium in

5 synchronism with a clock signal, it is necessary to adjust the phase of the clock signal so that the best sampled values can be obtained.

A conventional clock adjustment apparatus for the data reproduction system estimates the phase

10 error of the clock signal by using a value (for example, a center value of the readout signal) calculated in the process of reproducing recorded data through the Viterbi algorithm so as to control the phase of the clock signal by using the phase

15 error.

According to such a conventional clock adjustment apparatus, the overall structure of the data reproduction system including the clock adjustment apparatus can be simplified.

20 On the other hand, the above-described data reproduction system requires a higher-speed clock signal because of a higher recording density of the recording medium.

However, the conventional clock adjustment

25 apparatus, which estimates the phase error of the clock signal by using the processed readout data through the Viterbi algorithm, has difficulty in obtaining such a higher-speed clock signal necessary to guarantee the sampling of the readout signal at

30 the right phase.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a clock adjustment apparatus

35 for a data reproduction system and an apparatus having a data reproduction system including such a clock adjustment apparatus in which the above

disadvantages are eliminated.

A more specific object of the present invention is to provide a clock adjustment apparatus for a data reproduction system, which clock

5   adjustment apparatus produces a clock signal fast enough to guarantee sampling of a readout signal at the right phase, and an apparatus having a data reproduction system including such a clock adjustment apparatus.

10   The above-mentioned objects of the present invention are achieved by a clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal

15   from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, the recording medium being recorded with the data modulated in accordance with a

20   recording rule of a predetermined partial response characteristic, the clock adjustment apparatus including a phase error calculation circuit calculating the phase error of the clock signal based on the sampled values of the readout signal.

25   According to the above-mentioned data reproduction system, the waveform of the readout signal from the recording medium depends on the predetermined PR characteristic. When such a readout signal is sampled in synchronism with the

30   clock signal of the right phase, the transition state of the sampled values also depends on the PR characteristic. Therefore, the phase error of the clock signal can be obtained based on the extent of the difference between the transition state of the

35   sampled values obtained in synchronism with the clock signal and the transition state of expected sampled values corresponding to the PR

characteristic.

The above-mentioned objects of the present invention are also achieved by a clock adjustment apparatus for adjusting a phase of a clock signal

5 based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the

10 readout signal, the recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, the clock adjustment apparatus including a phase error calculation circuit

15 calculating the phase error of the clock signal based on a transition state of the sampled values of the readout signal before undergoing the Viterbi algorithm.

The above-mentioned objects of the present

20 invention are further achieved by an apparatus including a data reproduction system which samples a readout signal from a recording medium in synchronism with a clock signal, and reproduces data in accordance with a Viterbi algorithm by using

25 sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, the data reproduction system having a clock adjustment

30 circuit including a phase error calculation circuit calculating a phase error of the clock signal based on the sampled values of the readout signal, and adjusting a phase of the clock signal based on the phase error.

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BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of

the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing a structure of an optical disk apparatus according to an embodiment of the present invention;

FIG. 2 is a block diagram showing a structure of a readout system unit of the optical disk apparatus of FIG. 1;

FIG. 3 is a block diagram showing a structure of a phase error detection unit of the readout system unit of FIG. 2;

FIG. 4 is a block diagram showing a structure of a phase error detection circuit of the phase error detection unit of FIG. 3;

FIG. 5 is a diagram showing a waveform of a readout signal before being supplied to a Viterbi detection module so as to illustrate a phase error determined from an equation;

FIGS. 6(a), (b), (c) are a diagram for illustrating a threshold defined so as to prevent a wrong portion of the readout signal from being detected as an edge portion;

FIGS. 7(a), (b), (c) are a diagram for illustrating a masking threshold;

FIG. 8 is a block diagram showing a structure of an edge detection circuit of the phase error detection unit of FIG. 3;

FIG. 9 is a diagram showing a convergence process of the phase error of a clock signal according to the present embodiment;

FIG. 10 is a timing chart illustrating a switching of sampled values of the readout signal employed to detect the phase error; and

FIG. 11 is a diagram illustrating normalization of a phase error output.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given, with reference to the accompanying drawings, of an
5   embodiment of the present invention.

FIG. 1 shows a structure of an optical disk apparatus according to the embodiment of the present invention. The optical disk apparatus is a magneto-optical disk apparatus employing a magneto-
10   optical disk as a recording medium.

According to FIG. 1, the magneto-optical disk apparatus includes a magneto-optical disk 10 serving as a recording medium, an optical head 20, an amplifier 21, a readout system unit 25, a writing
15   system unit 26, an electromagnet 27, a control unit (MPU) 28, a servo system unit 29, and a motor 30. Data is recorded on the magneto-optical disk 10 in accordance with the recording rule of a predetermined PR characteristic (for example, the PR
20   (1, 1) of a constraint length 2), and is reproduced from the magneto-optical disk 10.

The MPU 28 controls the readout system unit 25, the writing system unit 26 and the servo system unit 29 in accordance with a data readout
25   command and a data writing command provided from an external unit (not shown) through a connector 32 and an interface circuit 31. A description will be given later of the control of the MPU 28 over the readout system unit 25.

30   According to the above-described magneto-optical disk apparatus, the optical head 20 optically scans the magneto-optical disk 10 when the data readout command is provided thereto, so that a readout signal output from the optical head 20 is
35   provided to the readout system unit 25 through the amplifier 21. The readout system unit 25 quantizes the provided readout signal and generates output

data from the quantized data in accordance with a
maximum likelihood (ML) decoding algorithm (for
example, the Viterbi algorithm). The output data is
provided to the MPU 28 and is further output
5   therefrom to the external unit through the interface
circuit 31 and the connector 32.

On the other hand, when the MPU 28
receives the data writing command as well as data to
be recorded from the external unit, the MPU 28
10   modulates the data in accordance with the
predetermined recording rule (for example, the PR (1,
1)), and provides the modulated data to the writing
system unit 26. The writing system unit 26 controls
the operation of the optical head 20 in accordance
15   with the modulated data, and the MPU 28 controls the
electromagnet 27 in accordance with data obtained
from the modulation of the data. As a result, the
data is written on the magneto-optical disk 10 in
accordance with the above-mentioned predetermined
20   recording rule.

The servo system unit 29, which is
controlled by the MPU 28, actuates the motor 30 so
as to rotate the magneto-optical disk 10 at a
predetermined speed, and positions the optical head
25   20 at the recording/reproduction position of the
magneto-optical disk 10.

FIG. 2 shows a structure of the above-
described readout system unit 25.

According to FIG. 2, the readout system
30   unit 25 includes a low-pass filter (LPF) 22, an
analog-to-digital converter (ADC) 23, a digital
equalizer (EQ) 24, a Viterbi detection module 100,
and a clock generation circuit 200.

The readout signal amplified by the
35   amplifier 21 shown in FIG. 1 is subjected to
waveform shaping at the LPF 22. The analog readout
signal output by the LPF 22 is sampled periodically

by the ADC 23. The ADC 23 converts the readout
signal into a digital-form readout signal in
synchronism with a clock signal supplied from the
clock generation circuit 200. In other words, the
5   above-mentioned readout signal is quantized by being
sampled by the ADC 23 operating in synchronism with
the clock signal.

The ADC 23 continuously samples the
readout signal in synchronism with the clock signal
10   generated from the clock generation circuit 200, and
outputs the digitized readout signal. The EQ 24
performs waveform equalization on the sampled values
of the digitized readout signal, so that the sampled
values are output as equalized output data
15   (quantized data). The equalized output data from
the EQ 24 is provided to the Viterbi detection
module 100 in synchronism with the above-mentioned
clock signal. The Viterbi detection module 100
detects, in accordance with the Viterbi algorithm,
20   the recorded data from the equalized output data
provided in synchronism with the clock signal, and
outputs the recorded data as reproduced data. In
the data reproduction system of FIG. 1, the EQ 24
and the Viterbi detection module 100 also operate in
25   synchronism with the clock signal supplied by the
clock generation circuit 200, although this is not
indicated in FIGS. 1 and 2.

Like generally used Viterbi detectors, the
above-mentioned Viterbi detection module 100
30   includes a branch metric calculation unit (BM) 101,
an add-compare-select unit (ACS) 102, a path metric
memory (PMM) 103, and a path memory (PM) 104.

The BM 101 calculates branch metrics which
corresponds to the differences between sampled
35   values and expected values which the readout signal
should take depending on the PR characteristic. The
ACS 102 adds previously calculated path metrics

stored in the PMM 103 to the corresponding above-mentioned branch metrics. The ACS 102 then compares each given pair of the calculated path metrics so as to select the smaller of the two. The selected path
5 metrics are stored in the PMM 103 as new path metrics. According to the above-described calculation, a path metric is expressed as an addition of branch metrics.

Selecting the smaller path metric as
10 described above corresponds to selecting a state transition path in the Viterbi algorithm. That is to say, the ACS 102 always selects a path so as to minimize the path metric. The ACS 102 supplies the PM 104 with binary data corresponding to the path
15 selected in the above-described way. In the PM 104 data corresponding to each of the selected paths is shifted, while discarding data corresponding to each of non-selected paths. As a result, data corresponding to each of the surviving paths is
20 output from the PM 104 as output data. Thus, the data recorded with high density on the magneto-optical disk 10 can be reproduced with high accuracy by recording the data in a PR waveform and detecting the maximum likelihood data by the Viterbi detection
25 module 100.

The above-mentioned clock generation circuit 200, serving as a feedback loop, includes a phase error detection unit (PED) 230 serving as a means for detecting a phase error, a digital-to-
30 analog converter (DAC) 240 and a phase-locked loop (PLL) 250.

As will be described later, the PED 230 detects the phase error of the above-mentioned clock signal on the basis of the sampled values of the
35 digitized readout signal obtained before undergoing the Viterbi detection module 100. First sampled values S1, which are quantized by the ADC 23 but not

subjected to the waveform equalization performed by the EQ 24, and second sampled values S2, on which the waveform equalization is performed by the EQ 24, are provided to the PED 230 in order to detect the

5   phase error of the clock signal.

The phase error of the clock signal detected by the PED 230 is converted into a corresponding voltage level (an analog value) by the DAC 240. The PLL 250, which includes a loop filter

10   (LF) and a voltage-controlled oscillator (VCO), controls the phase of the clock signal so as to reduce the phase error, based on the corresponding voltage level provided from the DAC 240. The clock signal, of which the phase is adjusted by the PLL

15   250, is provided to the ADC 23 sampling the readout signal.

FIG. 3 is a block diagram showing a structure of the PED 230 shown in FIG. 2. Also shown in FIG. 3 is the above-described MPU 28

20   inputting a plurality of control signals to the PED 230.

The PED 230 operates in two detection (operation) modes, namely, an acquisition mode and a tracking mode, to detect the phase error of the

25   clock signal. The acquisition mode is an initial adjustment mode, where the phase of the clock signal is adjusted, by using a VFO region arranged on a leading portion of each of the tracks of the magneto-optical disk 10, so that the sampling of the

30   readout signal is properly performed. In the acquisition mode, it is preferable to adjust the phase of the clock signal quickly by setting a gain to a high (Hi) state. A continuous repeat pattern modulated in accordance with the PR characteristic

35   is recorded on the above-mentioned VFO region, and the phase error of the clock signal can be reduced by adjusting the phase thereof in accordance with

the repeat pattern.

On the other hand, in the tracking mode, the phase error is gradually controlled by setting the gain to a low (Low) state after the phase of the
5 clock signal is adjusted in the acquisition mode to reduce the phase error. The tracking mode is employed in a data recording (DATA) region, on which is recorded a data signal obtained by modulating desired data in accordance with the PR
10 characteristic.

The PED 230 includes a multiplexer (MUX) 231, a phase error detection (calculation) circuit 233, an edge detection circuit 235, an OR circuit 236, an AND circuit 237, a gain adjustment circuit
15 238, and an AND circuit 239. The PED 230 detects the phase error of the clock signal in accordance with the control signals input from the MPU 28.

The first and second sampled values S1 and S2 output successively after being digitized in the
20 ADC 23 and equalized in the EQ 24, respectively, are input to the MUX 231. The MPU 28 inputs a sampled value selection signal 40 to the MUX 231 so that the MUX 231 outputs the first sampled values S1 in the acquisition mode and the second sampled values S2 in
25 the tracking mode. In the tracking mode, by employing the equalized second sampled values S2, the phase error of the clock signal can be calculated based on the sampled values of the readout signal having a waveform closer to that to
30 be reproduced. The MPU 28 inputs to the OR circuit 236 a mode selection signal 42 "1" when the phase error is output at all the sampling instants and a mode selection signal 42 "0" when the phase error is output only at edge portions of the data signal.
35 Thus, the MPU 28 serves as an operation mode switching circuit.

The phase error detection circuit 233

calculates the phase error of the clock signal in accordance with a below-described predetermined calculation process in the acquisition and tracking modes, and outputs a corresponding signal to the AND

5   circuit 237. The edge detection circuit 235 detects a rising edge portion or a falling edge portion of the recorded data of the readout signal in the tracking mode, and outputs a corresponding signal, which is input to the AND circuit 237 via the OR

10   circuit 236.

         The output signals from the phase error detection circuit 233 and the edge detection circuit 235 are supplied to the AND circuit 237. The AND circuit 237 produces an output signal corresponding

15   to the supplied signals, and outputs the corresponding signal to the gain adjustment circuit 238. At this point, the MPU 28 inputs a gain setting signal 44 to the gain adjustment circuit 238 so that the gain is set to the Hi state in the case

20   of the acquisition mode and to the Low state in the case of the tracking mode. That is, the MPU 28 switches the states of the gain, serving as a gain switching circuit.

         The PED 230 generally operates as follows.

25   First, in the acquisition mode, the first sampled values S1 are input to the phase error detection circuit 233 via the MUX 231. The phase error detection circuit 233 calculates the phase error of the clock signal from the first sampled values S1 in

30   accordance with the predetermined calculation process, and outputs the corresponding signal to the AND circuit 237. At the same time, the output signal from the MUX 231 is also supplied to the edge detection circuit 235. Since the mode selection

35   signal 42 "1" is continuously input from the MPU 28 to the OR circuit 236 in the acquisition mode, the output signal from the phase error detection circuit

233 is input to the gain adjustment circuit 238
through the AND circuit 237 in the acquisition mode.
In other words, the phase error of the clock signal
is continuously detected based on the successive
5   sampled values obtained at the upper peaks (the
maximum values), the lower peaks (the minimum
values), the rising edge portions, the falling edge
portions, and the center points between the upper
and lower peaks of the readout signal having the
10   highest density. Therefore, the phase error is so
frequently obtained that the phase of the clock
signal can be adjusted more quickly. The output
signal from the AND circuit 237 is adjusted to have
the gain set to the Hi state (hereinafter a Hi gain)
15   by the gain adjustment circuit 238, and is output
therefrom as the phase error.

        The signal output from the gain adjustment
circuit 238 as the phase error is supplied to the
DAC 240 shown in FIG. 2 via the AND circuit 239.
20   The AND circuit 239 is controlled by a masking
signal 46 output from the MPU 28, which will be
described later. When a low-level masking signal is
supplied to the AND circuit 239, the signal output
from the gain adjustment circuit 238 as the phase
25   error is masked and is not provided to the DAC 240.

        On the other hand, in the tracking mode,
the second sampled values S2 are input to the phase
error detection circuit 233 as well as to the edge
detection circuit 235 through the MUX 231. The
30   phase error detection circuit 233 calculates the
phase error of the clock signal from the second
sampled values S2 in accordance with the
predetermined calculation process, and outputs the
corresponding signal to the AND circuit 237. The
35   edge detection circuit 235 performs a predetermined
edge detection process, which will be described
later, on the second sampled values S2. The edge

detection circuit 235 outputs an edge detection signal "1" when determining that the second sampled values S2 are sampled at edge portions of the readout signal, and, when not, outputs an edge

5 detection signal "0". The detection signal is supplied to the OR circuit 236, to which the mode selection signal 42 "0", which indicates that the PED 230 is in the tracking mode, is input from the MPU 28. Therefore, when the edge detection signal

10 "1" is supplied to the OR circuit 236, the output signal from the phase error detection circuit 233 passes through the AND circuit 237 and is output to the gain adjustment circuit 238. Thus, the phase error of only the edge portions of the readout

15 signal is supplied to the gain adjustment circuit 238. The output signal from the AND circuit 237 is adjusted to have the gain set to the Low state (hereinafter a Low gain) by the gain adjustment circuit 238, and is output therefrom. The Low gain

20 is smaller than the Hi gain.

By thus adjusting the gain with respect to the phase error calculated by the phase error detection circuit 233 in accordance with the gain setting signal 44 from the MPU 28, the phase of the

25 clock signal can be adjusted so as to quickly shift close enough to its right phase in the acquisition mode and to be stable without oscillation in the tracking mode.

A description will now be given, with

30 reference to the accompanying drawings, of the calculation of the phase error of the clock signal performed by the phase error detection circuit 233. FIG. 4 is a block diagram showing a structure of the phase error detection circuit 233.

35 Suppose in FIG. 4 that a first sampled value Y_t at a sampling instant t, a second sampled value Y_{t-1} at a sampling instant t-1, which is

previous to the sampling instant t, and a third
sampled value Y_{t-2} at a sampling instant t-2, which
is previous to the sampling instant t-1, are input
in the order sampled to the phase error detection
5   circuit 233.

The phase error detection circuit 233
includes flip-flops (FF) 331 and 332, subtracters
333, 334 and 339, code determination circuits 335
and 336, and multipliers 337 and 338. The sampled
10   values Y_{t-1} and Y_{t-2} are simultaneously set in the FFs
331 and 332, respectively when the sampled value Y_t
is detected at the sampling instant t.

The phase error detection circuit 233
calculates the phase error (PE) of the clock signal
15   based on the following equation:

$$PE = (Y_t - Y_{t-1}) \times hat_{t-1, t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t, t-1}$$

20   where $hat_{t, t-1}$ = 1, 0, -1 in the cases of $Y_t - Y_{t-1} > 0$,
$Y_t - Y_{t-1} = 0$, $Y_t - Y_{t-1} < 0$, respectively, and $hat_{t-1, t-2}$ =
1, 0, -1 in the cases of $Y_{t-1} - Y_{t-2} > 0$, $Y_{t-1} - Y_{t-2} = 0$,
$Y_{t-1} - Y_{t-2} < 0$, respectively.

Since the waveform of the sampled readout
25   signal has the upper and lower peaks, and the center
points therebetween, the above equation is provided
with a ternary code "hat" to correct the transition
direction of the waveform so that the proper phase
error can be detected at any of the above points.
30   The first sampled value Y_t and the second
sampled value Y_{t-1} set in the FF 331 are input to the
subtracter 333, which subtracts Y_{t-1} from Y_t to
calculate a first difference. At the same time, the
second sampled value Y_{t-1} set in the FF 331 and the
35   third sampled value Y_{t-2} set in the FF 332 are input
to the subtracter 334, which subtracts Y_{t-2} from Y_{t-1}
to calculate another first difference. The first

difference calculated by the subtracter 333 is
output to the code determination circuit 335. The
code determination circuit 335 determines the
ternary code for the first difference calculated by
5   the subtracter 333, or determines hat$t, t-1$, and
outputs hat$t, t-1$ to the multiplier 338.
Simultaneously, the first difference calculated by
the subtracter 334 is output to the code
determination circuit 336. The code determination
10   circuit 336 determines the ternary code for the
first difference calculated by the subtracter 334,
or determines hat$t-1, t-2$, and outputs hat$t-1, t-2$ to the
multiplier 337. The product of Y_t-Y_{t-1} and hat$t-1, t-2$
calculated by the multiplier 337 and the product of
15   $Y_{t-1}-Y_{t-2}$ and hat$t, t-1$ calculated by the multiplier 338
are output to the subtracter 339. The subtracter
339 finally determines the phase error of the clock
signal from the above equation. In other words, the
subtracter 339 uses the absolute values of the two
20   first differences, which are calculated by
multiplying each of the two first differences by the
ternary code "hat" to correct the transition
direction, so as to calculate the difference between
the two absolute values from the above equation (a
25   second difference), which is equal to the phase
error of the clock signal.
        FIG. 5 shows a waveform of a readout
signal R before being supplied to the Viterbi
detection module 100 so as to illustrate the phase
30   error determined from the above equation. The
readout signal R is sampled in synchronism with the
clock signal to provide sampled values Y. The ideal
sampling of the readout signal R is performed by
generating the clock signal at the sampling instants
35   t, t-1 and t-2 corresponding to the lower peak, the
center point and the upper peak, respectively, of
the waveform, shown circled in FIG. 5. If the

readout signal R is sampled at the ideal sampling
instants t, t-1 and t-2, the phase error (PE) is
given by the above formula as follows:

5      $$PE = (Y_t - Y_{t-1}) \times hat_{t-1, t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t, t-1}$$
$$= (-1) \times (-1) - (-1) \times (-1)$$
$$= 1 - 1$$
$$= 0$$

10

Thus, it can be confirmed that there
exists no phase error.

Next, a description will be given of a
case where a phase error exists using FIG. 5. The
15 sampling of the readout signal is performed by
generating the clock signal at the sampling instants
T, T-1 and T-2, which deviate from the lower peak,
the center point and the upper peak, respectively.
The waveform is marked with a triangle at each of
20 the sampling instants T, T-1 and T-2.

Suppose that $Y_T = 0.1$, $Y_{T-1} = 0.7$ and $Y_{T-2} = 1.9$, the phase error (PE) is given by the above
equation as follows:

25     $$PE = (Y_t - Y_{t-1}) \times hat_{t-1, t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t, t-1}$$
$$= (0.1 - 0.7) \times (-1) - (0.7 - 1.9) \times (-1)$$
$$= 0.6 - 1.2$$
30     $$= -0.6$$

It is concluded from the above calculation
result that the clock signal lags behind by the
phase error of 0.6. Consequently, the phase of the
35 clock signal is controlled so as to correct the
above phase error. According to the above example,
the phase error is calculated with respect to the

falling edge portion including the center point. On
the other hand, the phase error can also be
calculated with respect to a rising edge portion
including a center point, or to an edge portion
5   including an upper or a lower peak. The first
differences Y_t-Y_{t-1} and $Y_{t-1}-Y_{t-2}$, that is, the
differences between the real sampled values, are
multiplied by the ternary codes $hat_{t-1, t-2}$ and $hat_{t, t-1}$, respectively, to correct the transition direction.
10 As a result, the absolute values of the first
differences are determined so that the phase error
can correctly be calculated based on the first
differences irrespective of the sampling instants at
which the readout signal is sampled. The difference
15 of the absolute values of the first differences is
determined from the above equation as the second
difference, which is employed as the phase error to
control the phase compensation.

A description will now be given, with
20 reference to FIGS. 6 through 8, of the edge
detection in the tracking mode performed by the edge
detection circuit 235. The edge detection is
provided in order to prevent the phase of the clock
signal from shifting from that of the readout signal
25 at the edge portions thereof when the readout signal
is reproduced from a storage medium which is likely
to cause the distortion of the waveform of the
readout signal at the edge portions thereof. The
edge detection circuit 235 detects the rising edge
30 portions or the falling edge portions based on the
sampled values obtained in the order sampled. Just
as previously described, suppose that the first,
second and third sampled values Y_t, Y_{t-1} and Y_{t-2} are
obtained at the sampling instants t, t-1 and t-2,
35 respectively. The conditions for detecting the
rising edge portions are established as $Y_{t-1}-Y_{t-2} > 0$
and $Y_t-Y_{t-1} > 0$.

Since the readout signal sampled in the
tracking mode is a data signal, a wrong portion of
the readout signal may be detected as an edge
portion because of the variation in the recorded
5   data thereof. Therefore, it is preferable to define
a threshold T so as to prevent a wrong portion of
the readout signal from being detected as an edge
portion. In the case of the rising edge portions,
the detection of a wrong portion can be precluded by
10   setting the following conditions: the third sampled
value Y_{t-2} is smaller than the threshold T ($Y_{t-2} < T$)
and the first sampled value Y_t is larger than the
threshold T ($Y_t > T$). Under these conditions, FIG.
6 (a) is detected as a rising edge portion, while
15   FIG. 6 (b) and (c) are not. The threshold T is
defined, for example, by a control signal from the
MPU 28 serving as a threshold defining circuit. The
MPU 28 suitably defines the threshold T depending on
a type of storage medium. By thus setting the
20   conditions, the rising edge portions of the readout
signal can be detected based on a series of discrete
but successive sampled values in ascending order
from a value smaller than the threshold T to a value
larger than the threshold T.
25   Similarly, the conditions for preventing
the detection of a wrong portion can be established
with respect to the falling edge portions. In the
case of the falling edge portions, the conditions
are opposite to those in the case of the rising edge
30   portions. In other words, the conditions are set as
follows: $Y_{t-1}-Y_{t-2} < 0$ and $Y_t-Y_{t-1} < 0$, and the third
sampled value Y_{t-2} is larger than the threshold T
($Y_{t-2} > T$) and the first sampled value Y_t is smaller
than the threshold T ($Y_t < T$).
35   Further, an asymmetric waveform should be
considered in the case of detecting edge portions of
a data signal. For example, a waveform of sampled

values of a data signal shown in FIG. 7 (a) includes
oval-circled portions each including three
successive sampled values. In this case, each of
the oval-circled portions can be detected as a
falling edge portion based on the above conditions
for preventing the wrong detection. If detected in
this way, pairs of successive falling edge portions
are indicated in a waveform indicating the edge
portions of the data signal as shown in FIG. 7 (b).
In order to prevent this, it is preferable to
perform a masking where a difference between two
successive sampled values is masked if the absolute
value thereof is smaller than a given value (defined
as a masking threshold mT). The masking threshold
mT can be defined, for example, based on a control
signal from the MPU 28.

A preferred waveform indicating the edge
portions of the data signal as shown in FIG. 7 (c)
is obtained by masking the first difference $Y_{t-1}-Y_{t-2}$
if $| Y_{t-1}-Y_{t-2} | < mT$ or the first difference Y_t-Y_{t-1}
if $| Y_t-Y_{t-1} | < mT$.

The threshold T is normally a fixed value
defined by the MPU 28. In some cases, a data signal
is offset in its amplitude direction by the envelope
variation thereof caused by the eccentricity of a
disk-shaped storage medium. Therefore, it is
preferable to perform the edge detection by adding
to the threshold T an estimated offset of the data
signal caused by the envelope variation thereof or
the like. In other words, it is desirable to add,
by an adder, the offset estimated by an offset
estimation circuit to the threshold T and input the
adding result thereof to the edge detection circuit
235. Thereby, the envelope variation of the data
signal can be considered in the edge detection, and
the threshold T is corrected in accordance with the
offset and can be maintained at the best level for

the edge detection.

FIG. 8 shows a structure of the edge
detection circuit 235, wherein the threshold T and
the masking threshold mT are defined with the offset
5   being considered.

According to FIG. 8, the edge detection
circuit 235 includes flip-flops (FF) 351 and 352, an
offset estimation circuit 353, an adder 354, and
subtracters 356 and 357. The sampled values Y_{t-1} and
10   Y_{t-2} are simultaneously set in the FFs 351 and 352,
respectively when the sampled value Y_t is detected
at the sampling instant t. The edge detection
circuit 235 further includes comparators 361 through
364 and AND circuits 375 and 377 for detecting a
15   rising edge portion, absolute value calculation
circuits 371 and 372, comparators 373 and 374, and
comparators 365 through 368 and AND circuits 376 and
378 for detecting a falling edge portion.

A description will now be given of the
20   detection of the rising edge portions. The
detection of the falling edge portions is performed
in the same process as the detection of the rising
edge portions by reversing almost all the conditions
for the detection of the rising edge portions.
25   Therefore, a detailed description thereof will be
omitted.

First, the first sampled value Y_t and the
second sampled value Y_{t-1} set in the FF 351 are input
to the subtracter 356, and at the same time, the
30   second sampled value Y_{t-1} set in the FF 351 and the
third sampled value Y_{t-2} set in the FF 352 are input
to the subtracter 357. The calculation result by
the subtracter 356 is output to the comparator 361,
which determines whether $Y_t - Y_{t-1} > 0$. If $Y_t - Y_{t-1} > 0$,
35   a value "1" is output to the AND circuit 375. If
$Y_t - Y_{t-1} \leq 0$, a value "0" is output to the AND
circuit 375. Simultaneously, the calculation result

of the subtracter 357 is output to the comparator 362, which determines whether $Y_{t-1} - Y_{t-2} > 0$. If $Y_{t-1} - Y_{t-2} > 0$, the value "1" is output to the AND circuit 375. If $Y_{t-1} - Y_{t-2} \leqq 0$, the value "0" is output to

5   the AND circuit 375. That is, a portion of the data signal including the above sampled values is detected as a probable rising edge portion when both of the comparators 361 and 362 output the values "1" to the AND circuit 375.

10   Next, it is determined whether the first and third sampled values Y_t and Y_{t-2} are above and below the threshold T defined by the MPU 28, respectively. The first sampled value Y_t and the threshold T defined by the MPU 28 are input to the

15   comparator 363. At this point, if the data signal has an offset, the threshold T defined by the MPU 28 is corrected by adding, by the adder 354, the offset estimated by the offset estimation circuit 353 thereto and the corrected threshold T is input to

20   the comparator 363. The comparator 363 compares the first sampled value Y_t and the threshold T. The comparator 363 outputs the value "1" to the AND circuit 375 if $Y_t > T$ and the value "0" if $Y_t < T$.

            At the same time, the comparator 364

25   compares the third sampled value Y_{t-2} and the threshold T. The comparator 364 outputs the value "1" to the AND circuit 375 if $Y_{t-2} < T$ and the value "0" if $Y_{t-2} > T$. That is, the portion of the data signal including the above-mentioned sampled values

30   is detected as a probable rising edge portion when both of the comparators 363 and 364 output the values "1" to the AND circuit 375.

            Next, a decision is made on the necessity of the masking based on the masking threshold mT

35   defined by the MPU 28. The calculation result of the subtracter 356 is also input to the absolute value calculation circuit 371. The absolute value

| Y_t-Y_{t-1} | calculated by the absolute value calculation circuit 371 and the masking threshold mT defined by the MPU 28 are input to the comparator 373. The comparator 373 compares | Y_t-Y_{t-1} | and the

5   masking threshold mT. The comparator 373 outputs the value "1" to the AND circuit 375 if | Y_t-Y_{t-1} | > mT and the value "0" if | Y_t-Y_{t-1} | ≦ mT. Therefore, if | Y_t-Y_{t-1} | ≦ mT, the first difference Y_t-Y_{t-1} is masked and the portion of the data signal including

10   the above-mentioned sampled values is not detected as a rising edge portion. Simultaneously, the calculation result of the subtracter 357 is also input to the absolute value calculation circuit 372. The absolute value | $Y_{t-1}-Y_{t-2}$ | calculated by the

15   absolute value calculation circuit 372 and the masking threshold mT defined by the MPU 28 are input to the comparator 374. The comparator 374 compares | $Y_{t-1}-Y_{t-2}$ | and the masking threshold mT. The comparator 374 outputs the value "1" to the AND

20   circuit 375 if | $Y_{t-1}-Y_{t-2}$ | > mT and the value "0" if | $Y_{t-1}-Y_{t-2}$ | ≦ mT. Therefore, if | $Y_{t-1}-Y_{t-2}$ | ≦ mT, the first difference $Y_{t-1}-Y_{t-2}$ is masked and the portion of the data signal including the above-mentioned sampled values is not detected as a rising

25   edge portion.

      The AND circuit 375, to which the above input signals are transmitted, outputs the value "1" to the AND circuit 377 only when all the input signals are the value "1", which indicates that the

30   portion of the data signal including the above-mentioned sampled values is detected as a rising edge portion. In the case of selecting a rising edge portion, the MPU 28 supplies a rising edge selection signal "1" to the AND circuit 377, which

35   outputs a corresponding signal to an OR circuit 379.

      The detection of the falling edge portions proceeds similarly through the comparators 365

through 368, the absolute value calculation circuits 371 and 372, the comparators 373 and 374, and the AND circuit 376. In the case of selecting a falling edge portion, the MPU 28 supplies a falling edge

5   selection signal "1" to the AND circuit 378, which outputs a corresponding signal to the OR circuit 379. Therefore, when a rising or a falling edge portion is detected, the OR circuit outputs the edge detection signal. In other words, the edge

10 detection circuit 235 shown in FIG.3 outputs the edge detection signal "1" to the OR circuit 236.

FIG. 9 shows a convergence process of the phase error of the clock signal according to the present embodiment. A waveform 400 indicates the

15 output level of the phase error. The MPU 28 determines a timing for switching the acquisition and tracking modes by making a judgment on the state of convergence of the phase error of the clock signal. The timing can be determined depending on

20 the characteristic of a storage medium by the MPU 28 serving as a convergence time setting circuit. The convergence of the phase error is determined when the amplitude of a detected phase error output remains within a predetermined range for a

25 predetermined period of time, namely, for a longer period than a predetermined reference time length set by the MPU 28. The MPU 28 functioning as a convergence range setting circuit can also set the predetermined range. The acquisition mode can

30 smoothly be switched to the tracking mode after it is determined that the phase error converges within the predetermined range according to the above judgment on the convergence state thereof.

As the MPU 28 can make the above judgment

35 on the convergence state of the phase error, the MPU 28 can automatically switch the acquisition mode to the tracking mode by outputting the mode selection

signal 42 to the OR circuit 236 when the convergence
of the phase error within the predetermined range is
determined. Further, the gain setting signal 44
input to the gain adjustment circuit 238 from the
5   MPU 28 can be set so as to automatically switch the
state of the gain from Hi to Low, simultaneously
with the above-mentioned mode switching, after the
convergence of the phase error within the
predetermined range is confirmed. A dotted waveform
10   410 in FIG. 9 shows a waveform which the phase error
takes if the gain is maintained in the original
state, that is, the Hi state, without being switched
to the Low state. As can be seen from the
comparison between the waveform 400 and the dotted
15   waveform 410, the range of the amplitude of the
phase error narrows faster with the Low gain than
the Hi gain after the convergence of the phase error
within the predetermined range is determined.
In FIG. 9, the predetermined range of the
20   amplitude of the phase error is set between a first
output level H and a second output level L. When
the amplitude of the phase error detected by the
phase error detection circuit 233 falls within the
above-mentioned predetermined range, a timer
25   operation is started to count the time length
required for the phase error to shift between the
first and second output levels H and L. When the
time length is shorter than a reference time length,
the mode switching does not occur. On the other
30   hand, when the time length is longer than the
reference time length, the mode switching occurs.
For example, in the case of a time length C1 in FIG.
9, which is shorter than a predetermined reference
time length C, the mode switching does not occur and
35   the acquisition mode is maintained. On the other
hand, in the case of a time length C2, which is
longer than the predetermined reference time length

C, the mode is switched from the acquisition mode to the tracking mode and the state of the gain is switched from Hi to Low when the time length for which the phase error remains between the first and
5   second output levels H and L becomes longer than the reference time length C. Thereafter, the tracking mode is maintained. As previously described, when the amplitude of the phase error of the clock signal remains within the predetermined range for the
10   predetermined period of time in the acquisition mode, the convergence of the phase error is determined, that is, it is determined that the phase of the clock signal shifts close enough to its right phase. Then, the tracking mode begins and the phase of the
15   clock signal is adjusted based on the sampled values of the readout signal obtained at the edge portions thereof, so that the phase thereof is prevented from getting out of a predetermined range in the tracking mode.
20   FIG. 10 illustrates the switching of the sampled values of the readout signal employed to detect the phase error from the first sampled values S1 to the second sampled values S2. As previously described, the first sampled values S1 output from
25   the ADC 23 are employed to calculate the phase error in the acquisition mode, while the second sampled values S2 output from the EQ 24 are employed in the tracking mode. Although the second sampled values S2 may be employed both in the acquisition and
30   tracking modes, it is desirable to employ the first sampled values S1 in the acquisition mode to quickly adjust the phase of the clock signal. By thus selectively employing the two types of the sampled values S1 and S2 before going through the Viterbi
35   detection circuit 100, the phase of the clock signal can efficiently be controlled with respect to the real sampled values obtained through the PRML method.

However, the first and second sampled
values S1 and S2 are employed in parallel with each
other to calculate the phase error at one point
during the mode switching from the acquisition mode
5   to the tracking mode, due to a delay in outputting
the sampled values S2 resulting from the waveform
equalization thereon by the EQ 24. As previously
described, the sampling conditions of the
acquisition and tracking modes differ considerably
10   from each other. Therefore, if the phase error
output during the mode switching is employed, the
phase of the clock signal may wrongly be adjusted.
Hence, according to the present embodiment, the
phase error output is masked by the masking signal
15   46 for a predetermined period of time when the first
sampled values S1 are switched to the second sampled
values S2. Therefore, the adverse effect of the
above delay resulting from the waveform equalization
can be eliminated, and the phase of the clock signal
20   is prevented from being wrongly adjusted. According
to FIG. 10, the phase error output is masked for a
period M, during which the masking signal 46 is
supplied. More specifically, the masking signal 46
is supplied from the MPU 28 to the AND circuit 239
25   shown in FIG. 3 as a gate control signal.

As previously described, the sampled value
selection signal 40 switching the sampled value S1
to the sampled value S2 is output from the MPU 28.
As shown in FIG. 10, the gain state may be switched
30   from Hi to Low when a certain period of time passes
after the switching of the sampled values.

FIG. 11 is a diagram illustrating the
normalization of the phase error output. It is
desirable to set the gain based on the upper peak
35   (the maximum value) or the lower peak (the minimum
value) of the readout signal obtained at the end of
the acquisition mode, namely, the amplitude of the

readout signal, so that a gain $K\Phi$ in the transfer function of the clock generation circuit 200 remains constant. By thus adjusting the gain so that the peak-to-peak value of the amplitude of the phase

5 error output remains constant, the readout signal having different amplitudes can be processed without changing the constant of an integrator. The above gain adjustment process is performed by the gain adjustment circuit 238 shown in FIG. 3. In FIG. 11,

10 by being subjected to the above-mentioned gain adjustment process, the peak values of amplitude 500 of the phase error output are reduced to those of amplitude 510 thereof, of which the peak-to-peak value is equal to a predetermined constant peak-to-

15 peak value 520.

The present invention is not limited to the specifically disclosed embodiment, and variations and modifications may be made without departing from the scope of the present invention.

20 For example, according to the present embodiment, the present invention is applied to the magneto-optical disk as the recording medium. However, the present invention is not limited thereto, and may be applied to any medium from which

25 a signal can be optically read out and to an apparatus having a data reproduction system therefor.

The present application is based on Japanese priority application No. 11-361550 filed on December 20, 1999, the entire contents of which are

30 hereby incorporated by reference.